

726 A to Z of C

MEM 0040h:00CEh - COUNT OF DAYS SINCE LAST BOOT

Size: WORD

-----*-M004000D0-----

MEM 0040h:00D0h - RESERVED

Size: 32 BYTES

-----S-M004000D0-----

MEM 0040h:00D0h - Digiboard MV/4 - LENGTH OF DATA TABLE

Size: BYTE

-----d-M004000D0-----

MEM 0040h:00D0h EHD floppy - INSTALLATION FLAGS

Size: BYTE

Bitfields for EHD floppy installation flags:

Bit(s) Description (Table M0051)

4 installation completed

3-0 drives 0-3

-----b-M004000D0-----

MEM 0040h:00D0h - AMI BIOS v1.00.12.AX1T - EPP - SCRATCH SPACE

Size: WORD

Desc: this word holds the value of BX during an EPP BIOS call

SeeAlso: MEM 0040h:00D2h"AMI",MEM 0040h:00D5h"AMI",MEM 0040h:00D6h"AMI"

SeeAlso: MEM 0040h:00DDh"AMI"

-----S-M004000D1-----

MEM 0040h:00D1h - Digiboard MV/4 - PRODUCT ID

Size: BYTE

-----S-M004000D2-----

MEM 0040h:00D2h - Digiboard MV/4 - BASE ADDRESS FOUND

Size: WORD

-----b-M004000D2-----

MEM 0040h:00D2h - AMI BIOS v1.00.12.AX1T - EPP BASE I/O PORT

Size: WORD

-----S-M004000D4-----

MEM 0040h:00D4h - Digiboard MV/4 - PORTS

Size: BYTE

-----S-M004000D5-----

MEM 0040h:00D5h - Digiboard MV/4 - IRQ

Size: BYTE

-----d-M004000D5-----

MEM 0040h:00D5h - EHD floppy - NUMBER OF FLOPPY DISK CONTROLLERS IN SYSTEM

Size: BYTE

-----b-M004000D5-----

MEM 0040h:00D5h - AMI BIOS v1.00.12.AX1T - EPP - PARALLEL PORT 0 CAPABILITIES

Size: BYTE

SeeAlso: MEM 0040h:00D2h"AMI",MEM 0040h:00D6h"AMI",MEM 0040h:00D7h"AMI"

SeeAlso: MEM 0040h:00DCh"AMI"

-----d-M004000D6-----

MEM 0040h:00D6h - EHD floppy - AND-BITS TO ADJUST PORT ADDRESS

Size: BYTE

Note: this byte contains FFh if controller at 03Fyh and 7Fh if at 037yh; the value is ANDed with DL prior to using IN A?,DX or OUT DX,A? instructions

-----K-M004000D6-----

MEM 0040h:00D6h - Digiboard MV/4 - NUMBER OF KEYBOARDS FOUND

Size: WORD

SeeAlso: MEM 0040h:00D8h"Digiboard"

-----b-M004000D6-----

MEM 0040h:00D6h - AMI BIOS v1.00.12.AX1T - EPP - PARALLEL PORT 0 IRQ

Size: BYTE

SeeAlso: MEM 0040h:00D2h"AMI",MEM 0040h:00D5h"AMI",MEM 0040h:00D8h"AMI"

SeeAlso: MEM 0040h:00DDh"AMI"

-----d-M004000D7-----

MEM 0040h:00D7h - EHD floppy - DRIVE 0 DISKETTE MEDIA STATE

Size: BYTE

Note: the value in this byte is copied into 0040h:0090h (diskette 0 status)

SeeAlso: MEM 0040h:00D8h"EHD",MEM 0040h:00D9h"EHD",MEM 0040h:00DAh"EHD"

Bitfields for EHD diskette media state:

Bit(s) Description (Table M0052)

7-6 data rate: 00=500kbps,01=300kbps,10=250k,11=1M/S

5 double stepping required (e.g. 360kB in 1.2MB)

4 media type established

3 reserved

2-0 on exit from BIOS, contains:

000 trying 360kB in 360kB

001 trying 360kB in 1.2MB

010 trying 1.2MB in 1.2MB

011 360kB in 360kB established

100 360kB in 1.2MB established

101 1.2MB in 1.2MB established

110 reserved (2M8?)

111 all other formats/drives

-----b-M004000D7-----

MEM 0040h:00D7h - AMI BIOS v1.00.12.AX1T - EPP - PARALLEL PORT 1 CAPABILITIES

Size: BYTE

SeeAlso: MEM 0040h:00D2h"AMI",MEM 0040h:00D5h"AMI",MEM 0040h:00D6h"AMI"

SeeAlso: MEM 0040h:00DDh"AMI"

-----M-M004000D8-----

MEM 0040h:00D8h - Digiboard MV/4 - NUMBER OF MICE FOUND

Size: WORD

SeeAlso: MEM 0040h:00D6h"Digiboard",MEM 0040h:00DAh"Digiboard"

-----d-M004000D8-----

MEM 0040h:00D8h - EHD floppy - DRIVE 1 DISKETTE MEDIA STATE

Size: BYTE

SeeAlso: MEM 0040h:00D7h"EHD",MEM 0040h:00D9h"EHD",MEM 0040h:00DAh"EHD"

-----b-M004000D8-----

MEM 0040h:00D8h - AMI BIOS v1.00.12.AX1T - EPP - PARALLEL PORT 1 IRQ

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Size: BYTE

SeeAlso: MEM 0040h:00D2h"AMI",MEM 0040h:00D6h"AMI",MEM 0040h:00D7h"AMI"

SeeAlso: MEM 0040h:00DDh"AMI"

-----b-M004000D8-----

MEM 0040h:00D8h U - Phoenix BIOS 4.0 Rel 6.0 - POWER MANAGEMENT FLAGS

Size: BYTE

SeeAlso: INT 15/AX=5300h

-----d-M004000D9-----

MEM 0040h:00D9h - EHD floppy - DRIVE 2 DISKETTE MEDIA STATE

Size: BYTE

SeeAlso: MEM 0040h:00D7h"EHD",MEM 0040h:00D8h"EHD",MEM 0040h:00DAh"EHD"

-----S-M004000DA-----

MEM 0040h:00DAh - Digiboard MV/4 - CURRENT PORT (used by VGA initializatn only)

Size: BYTE

SeeAlso: MEM 0040h:00D8h"Digiboard"

-----d-M004000DA-----

MEM 0040h:00DAh - EHD floppy - DRIVE 3 DISKETTE MEDIA STATE

Size: BYTE

SeeAlso: MEM 0040h:00D7h"EHD",MEM 0040h:00D8h"EHD",MEM 0040h:00D9h"EHD"

-----S-M004000DB-----

MEM 0040h:00DBh - Digiboard MV/4 - MASTER 8259 MASK (used by VGA init only)

Size: BYTE

SeeAlso: MEM 0040h:00DCh"Digiboard"

-----d-M004000DB-----

MEM 0040h:00DBh - EHD floppy - DRIVE 0 NEEDS RECALIBARATION

Size: BYTE

SeeAlso: MEM 0040h:00DCh"EHD",MEM 0040h:00DDh"EHD",MEM 0040h:00DEh"EHD"

-----S-M004000DC-----

MEM 0040h:00DCh - Digiboard MV/4 - SLAVE 8259 MASK (used by VGA init only)

Size: BYTE

SeeAlso: MEM 0040h:00DBh"Digiboard"

-----b-M004000DC-----

MEM 0040h:00DCh - AMI BIOS v1.00.12.AX1T - EPP - PARALLEL PORT 0 MODE

Size: BYTE

SeeAlso: MEM 0040h:00D2h"AMI",MEM 0040h:00D5h"AMI",MEM 0040h:00DDh"AMI"

SeeAlso: INT 17/AX=0200h/BX=5050h

(Table M0053)

Values for AMI Enhanced Parallel Port mode:

01h compatibility mode

02h bi-directional mode

04h EPP mode

SeeAlso: #00637

-----d-M004000DC-----

MEM 0040h:00DCh - EHD floppy - DRIVE 1 NEEDS RECALIBARATION

Size: BYTE

SeeAlso: MEM 0040h:00DBh"EHD",MEM 0040h:00DDh"EHD",MEM 0040h:00DEh"EHD"

-----b-M004000DC-----

MEM 0040h:00DCh - AMI BIOS v1.00.12.AX1T - EPP - PARALLEL PORT 1 MODE
 Size: BYTE

SeeAlso: MEM 0040h:00D2h"AMI",MEM 0040h:00DCh"AMI",#M0053
 -----d-M004000DD-----

MEM 0040h:00DDh - EHD floppy - DRIVE 2 NEEDS RECALIBARATION
 Size: BYTE

SeeAlso: MEM 0040h:00DBh"EHD",MEM 0040h:00DCh"EHD",MEM 0040h:00DEh"EHD"
 -----d-M004000DE-----

MEM 0040h:00DEh - EHD floppy - DRIVE 3 NEEDS RECALIBARATION
 Size: BYTE

SeeAlso: MEM 0040h:00DBh"EHD",MEM 0040h:00DCh"EHD",MEM 0040h:00DDh"EHD"
 -----b-M004000DF-----

MEM 0040h:00DFh - AMI BIOS v1.00.12.AX1T - EPP - PARALLEL PORT LOCK STATE
 Size: BYTE

Note: set to 01h if last request was to lock a port, 00h if last request was
 to unlock a port

SeeAlso: MEM 0040h:00D2h"AMI",MEM 0040h:00DCh"AMI"
 -----b-M004000EO-----

MEM 0040h:00E0h - AMI BIOS v1.00.12.AX1T - EPP - REAL-TIME DEVICE COUNT
 Size: BYTE

Desc: contains the number of advertised real-time devices as set by EPP
 function 12h (see #00632)

SeeAlso: MEM 0040h:00D2h"AMI",MEM 0040h:00DFh"AMI"
 -----b-M004000EO-----

MEM 0040h:00E0h - Phoenix 386 BIOS - DRIVE PARAMETER TABLE FOR FIRST HARD DISK
 Size: 16 BYTES

Note: this area is used to store the driver parameter table for the first
 hard disk if it has been setup as the user-configurable "type 47"

-----d-M004000E3-----

MEM 0040h:00E3h - EHD floppy - DRIVE 0 DISKETTE TYPE (from jumpers)
 Size: BYTE

SeeAlso: MEM 0040h:00E4h,MEM 0040h:00E5h"EHD",MEM 0040h:00E6h"EHD"

(Table M0054)

Values for EHD floppy diskette type:

- 01h undefined by diskette change (360K)
- 02h 1.2M
- 03h 720K
- 04h 1.44M
- 05h 2.88M

-----d-M004000E4-----

MEM 0040h:00E4h - EHD floppy - DRIVE 1 DISKETTE TYPE (from jumpers)
 Size: BYTE

SeeAlso: MEM 0040h:00E3h,MEM 0040h:00E5h"EHD",MEM 0040h:00E6h"EHD"
 -----d-M004000E5-----

MEM 0040h:00E5h - EHD floppy - DRIVE 2 DISKETTE TYPE (from jumpers)
 Size: BYTE

SeeAlso: MEM 0040h:00E3h,MEM 0040h:00E4h"EHD",MEM 0040h:00E6h"EHD"

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MEM 0040h:00E5h - AWARD v4.51PG - ASSOC DRIVE NUMBERS TO PHYSICAL INTERFACES

Size: BYTE

SeeAlso: MEM 0040h:00B5h"Gigabyte"

Bitfields for drive number/interface mapping:

Bit(s) Description (Table M0128)

7-6 interface for drive 83h (F:)

00 primary master

01 primary slave

10 secondary master

11 secondary slave

5-4 interface for drive 82h (as for bits 7-6)

3-2 interface for drive 81h (as for bits 7-6)

1-0 interface for drive 80h (C:) (as for bits 7-6)

SeeAlso: #M0129

-----d-M004000E6-----

MEM 0040h:00E6h - EHD floppy - DRIVE 3 DISKETTE TYPE (from jumpers)

Size: BYTE

SeeAlso: MEM 0040h:00E3h, MEM 0040h:00E4h"EHD", MEM 0040h:00E5h"EHD"

-----d-M004000EA-----

MEM 0040h:00EAh - Omti controller - SEGMENT OF EXTENDED BIOS DATA AREA???

Size: WORD

Note: drive parameter tables stored in specified segment

-----b-M004000EC-----

MEM 0040h:00ECh - Dell 4xxDE BIOS A11 - LOOP COUNT FOR DELAYS

Size: WORD

-----M004000F0-----

MEM 0040h:00F0h - INTRA-APPLICATION COMMUNICATION AREA

Size: 16 BYTES

-----B-M00500000-----

MEM 0050h:0000h - PRINT-SCREEN STATUS

Size: BYTE

-----J-M00500001-----

MEM 0050h:0001h - NEC PC-9800 series - SCREEN MODE

Size: BYTE

Note: if bit 3 set, the screen is in high-resolution mode (start memory at segment E000h instead of A000h)

-----D-M00500004-----

MEM 0050h:0004h - MS-DOS - LOGICAL DRIVE FOR SINGLE-FLOPPY SYSTEM (A: / B:)

Size: BYTE

-----A-M0050000E-----

MEM 0050h:000Eh - STATE OF BREAK CHECKING AT START OF BASICA.COM EXECUTION

Size: BYTE

-----A-M0050000F-----

MEM 0050h:000Fh - BASICA VERSION FLAG

Size: BYTE

Note: this byte contains the value 02h if BASICA v2.10 is running

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-----A-M00500010-----
MEM 0050h:0010h - POINTER TO BASIC DATA SEGMENT
Size:  WORD
-----A-M00500012-----
MEM 0050h:0012h - INT 08 VECTOR AT START OF BASICA.COM EXECUTION
Size:  DWORD
-----A-M00500016-----
MEM 0050h:0016h - INT 1B VECTOR AT START OF BASICA.COM EXECUTION
Size:  DWORD
-----A-M0050001A-----
MEM 0050h:001Ah - INT 24 VECTOR AT START OF BASICA.COM EXECUTION
Size:  DWORD
-----D-M00600000-----
MEM 0060h:0000h - DOS 2+ SCRATCH SPACE
Size:  256 BYTES
Note:  used during DOS 2+ boot process
-----D-M00600000-----
MEM 0060h:0000h - DOS 1.x IO.SYS LOAD ADDRESS
-----D-M00700000-----
MEM 0070h:0000h - DOS 2+ IO.SYS LOAD ADDRESS
-----D-M00700100-----
MEM 0070h:0100h - DOS 5+ - ORIGINAL INTERRUPT VECTORS 10h,13h,15h,19h,1Bh
Size:  25 BYTES
Note:  each value is stored as a BYTE for the interrupt number followed by
       a DWORD for the vector
       these values are restored on INT 19 by recent versions of
       DR/Novell/PC/MS-DOS (MS-DOS 3.x used this area to support HIMEM.SYS)
       not supported by OS/2 MDOS
SeeAlso: MEM 0080h:0000h,INT 2F/AH=13
-----d-M0070016C-----
MEM 0070h:016Ch - DR-DOS 7.02-7.03 - "DEVNO" AUX/PRN PORT ASSIGNMENTS
Size:  2 BYTES

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016Ch BYTE PRN: assignment (0..2 for LPT1:..LPT3: (3 for LPT4:); default: 1)
016Dh BYTE AUX: assignment (0..3 for COM1:..COM4:; default: 1)

```

Notes: As long as the built-in AUX: or PRN: drivers are in effect, these settings can be transparently reassigned at the DR-OpenDOS 7.02 / DR-DOS 7.03 DOS BIOS device driver level (that is below DOS redirection etc., but above ROM BIOS) using the undocumented CONFIG.SYS AUX=0|1..4 and PRN=0|1..3|4 directive, where 1..4 specifies COM1:..COM4: or LPT1:..LPT4: and the high speed bypass 0 selects the previous hardwired equivalence of AUX: with COM1: and PRN: with LPT1: at this level, saving a few clock cycles. The system defaults to AUX=1 and PRN=1 (that is 0 in the internal variables). If the high speed bypass was not enabled, the assignment can be changed anytime later by updating these bytes, e.g. by a future issue of the MODE utility. If the highspeed bypass has been enabled, changes have

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no effect.

The LPT4 setting (or corresponding value 3) is valid for DR-OpenDOS 7.02 and DR-DOS 7.02, but due to a bug introduced with the partial removal of the LPT4: device, it must not be used under DR-DOS 7.03.

The address 0070h:016Ch is only valid for DR-OpenDOS 7.02 up to DR-DOS 7.03 (BDOS 73h), and will most probably change with future releases of DR-DOS!

These bytes are local for each task running.

SeeAlso: INT 21h/03h, INT 21h/04h, INT 21h/05h, MEM 0040h:0000h etc.

-----H-M00800000-----

MEM 0080h:0000h - 80286 CPU - LOADALL WORKSPACE

Size: 102 BYTES

Desc: on the 80286 (unlike 80386), the state buffer from which the LOADALL instruction loads all internal registers is hardwired to physical address 000800h

Note: several versions 3.x of MS-DOS leave an empty space at offset 100h in IO.SYS (which is loaded at 0070h:0000h) so that HIMEM.SYS can use LOADALL on 80286 machines without having to save/restore the area of memory that LOADALL uses

SeeAlso: MEM 0070h:0100h

-----m-m80C00000-----

MEM 80C00000h - Compaq Deskpro 386 system memory board register

Size: BYTE

80C00000 R Diagnostics register (see #M0055)

80C00000 W RAM relocation register (see #M0056)

Bitfields for Compaq Deskpro 386 diagnostics register:

Bit(s) Description (Table M0055)

7 =0 memory expansion board is installed

6 =0 second 1 MB of system memory board is installed

5-4 base memory

00 set to 640 KB

01 invalid

10 set to 512 KB

11 set to 256 KB

3 parity correct in byte 3

2 parity correct in byte 2

1 parity correct in byte 1

0 parity correct in byte 0 (in 32-bit double word)

SeeAlso: #M0056

Bitfields for Compaq Deskpro 386 RAM relocation register:

Bit(s) Description (Table M0056)

7-2 reserved, always write 1's.

1 =0 Write-protect 128-Kbyte RAM at FE0000.

=1 Do not write-protect RAM at FE0000.

0 =0 Relocate 128-Kbyte block at FE0000 to address 0E0000
 =1 128-Kbyte RAM is addressed only at FE0000.

SeeAlso: #M0055

-----m80C00000-----

MEM 80C00000h - COMPAQ DIAGNOSTICS REGISTER

Size: WORD

Note: Writing to F000h:FFE0h seems to involve unlocking the memory by writing FEFEh to this address first. The write-protection can be reestablished by writing FCFCh to this address???. This was seen done by MS HIMEM.SYS.

SeeAlso: F000h:FFE0h

Bitfields for Compaq Diagnostics Register:

Bit(s) Description (Table M0132)

15-10 unknown purpose (should remain set???)

9 =1 memory is read-write???
 =0 memory is read-only???

8 =1 to disable ROM replacement???
 =0 normal???

7-2 unknown purpose (should remain set???)

1 =1 memory is read-write
 =0 memory is read-only

0 =1 to disable ROM replacement???
 =0 normal

Note: Writing to F000h:FFE0h seems to involve unlocking the memory by writing FEFEh to this address first. The write-protection can be reestablished by writing FCFCh to this address???. Microsoft HIMEM.SYS was seen to do this.

SeeAlso: F000h:FFE0h

-----V-MA0000000-----

MEM A000h:0000h - EGA+ GRAPHICS BUFFER

Size: 65536 BYTES

-----V-MA0000000-----

MEM A000h:0000h - S3 - MEMORY-MAPPED GRAPHICS PROCESSOR REGISTERS

Size: 65536 BYTES

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

-----V-MA0001234-----

MEM A000h:1234h - S3 - MEMORY-MAPPED ???

Size: WORD???

Note: the Win95 driver for the Stealth64 tests various bits in this word, sometimes looping until a particular bit is set or cleared

-----V-MA0008000-----

MEM A000h:8000h - S3 - MEMORY-MAPPED PCI CONFIGURATION REGISTERS

Size: 256 BYTES

Notes: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear

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frame buffer

additional setup may be required to access these registers via memory

the DWORDs at 8080h,8088h,808Ch,8090h,8094h,8098h,809Ch are used by
STLTH64.DRV

the DWORDs at 18080h,18088h,18090h,18094h,18098h,1809Ch are written
by S3_32.DLL

-----V-MA0008100-----

MEM A000h:8100h - S3 - MEMORY-MAPPED PACKED REGISTERS

Size: 80 BYTES

Access: Write-Only

Desc: these registers pack two 16-bit I/O registers into a single DWORD
for faster writes

Note: the S3 graphics processor registers can be mapped at either
linear 000A0000h or at offset 16M from the start of the linear
frame buffer

SeeAlso: MEM A000h:8180h

Format of S3 Trio32/Trio64 packed memory-mapped registers:

Offset Size Description (Table M0057)

8100h	DWORD	drawing control: row (low word), column (high word) "CUR_X" and "CUR_Y" (see PORT 82E8h,PORT 86E8h)
8104h	DWORD	(Trio64) drawing control: row 2 (low word), column 2 (high word)
8108h	DWORD	drawing control: destination Y and axial step constant (low word), destination X and axial step constant (high word) (see PORT 8AE8h,PORT 8EE8h)
810Ch	DWORD	(Trio64 only) destination Y 2 and axial step constant 2 (low word), destination X 2 and axial step constant 2 (high word) (see PORT 8AEAh,PORT 8EEAh)
8110h	WORD	error term (see PORT 92E8h)
8112h	WORD	(Trio64) error term 2 (see PORT 92EAh)
8114h	DWORD	unused??? (would correspond to PORT 96E8h)
8118h	WORD	drawing control: command register (see PORT 9AE8h)
811Ah	WORD	(Trio64) command register 2 (see PORT 9AEAh)
811Ch	DWORD	short stroke (see PORT 9EE8h)
8120h	DWORD	background color (see PORT A2E8h)
8124h	DWORD	foreground color (see PORT A6E8h)
8128h	DWORD	write mask (see PORT AAE8h)
812Ch	DWORD	read mask (see PORT AEE8h)
8130h	DWORD	color compare (see PORT B2E8h)
8134h	DWORD	background mix (low word) and foreground mix (high word) (see PORT B6E8h,PORT BAE8h)
8138h	DWORD	top scissors (low word) and left scissors (high word) (see PORT BEE8h,#P1047)
813Ch	DWORD	bottom scissors (low word) and right scissors (high word) (see PORT BEE8h,#P1047)
8140h	DWORD	data manipulation control (low word) and miscellaneous 2 (high word) (see PORT BEE8h,#P1047)
8144h	DWORD	miscellaneous (low word) and read register select (high word)

(see PORT BEE8h,#P1047)

8148h DWORD minor axis pixel count (low word) and major axis pixel count
(high word) (see PORT BEE8h,#P1047,PORT 96E8h)

814Ch WORD (Trio64) major axis pixel count 2 (see PORT 96EAh)

8150h DWORD pixel data transfer (see PORT E2E8h,PORT E2EAh)

8154h 4 DWORDs ???

8164h DWORD ??? (written by STLTH64.DRV for Win95)

8168h DWORD (Trio64 only) Pattern Y (low word), Pattern X (high word)
(see PORT EAE8h,PORT EAEA)

816Ch DWORD ??? (written by STLTH64.DRV for Win95)

Note: setting 8138h to 0 and 813Ch to 12345678h may be a magic value to unlock
some S3 features

SeeAlso: #M0073,#M0070

-----V-MA0008180-----

MEM A000h:8180h - S3 - STREAMS PROCESSOR

Size: 128 BYTES

Note: the S3 graphics processor registers can be mapped at either
linear 000A0000h or at offset 16M from the start of the linear
frame buffer

SeeAlso: MEM A000h:8100h, MEM A000h:FF00h

Format of S3 Streams Processor memory-mapped registers:

Offset	Size	Description (Table M0058)
8180h	DWORD	primary stream control (see #M0059)
8184h	DWORD	chroma key control (see #M0063)
8188h	DWORD	unused??? (high word seems to echo 8184h, low word 8180h)
818Ch	DWORD	unused??? (high word seems to echo 8184h, low word 8180h)
8190h	DWORD	secondary stream control (see #M0061)
8194h	DWORD	chroma key upper bound (bits 23-0) (see also #M0063)
8198h	DWORD	secondary stream stretch (see #M0062)
819Ch	DWORD	??? (set by S3_32.DLL)
		bits 30-16: ???
		bits 14-0: ???
81A0h	DWORD	blend control (see #M0064)
81A4h	3 DWORDs	unused??? (reads as FFFFFFFFh)
81B0h	4 DWORDs	??? (appear to be read-only)
81C0h	DWORD	primary frame buffer address 0 (bits 21-0, multiple of 8)
81C4h	DWORD	primary frame buffer address 1 (bits 21-0, multiple of 8)
81C8h	DWORD	primary stream stride (bits 11-0 only)
81CCh	DWORD	double buffer/LPB control (see #M0065)
81D0h	DWORD	secondary frame buffer address 0 (bits 21-0, multiple of 8)
81D4h	DWORD	secondary frame buffer address 1 (bits 21-0, multiple of 8)
81D8h	DWORD	secondary stream stride (bits 11-0 only)
81DCh	DWORD	opaque overlay control (see #M0066)
81E0h	DWORD	K1 -- vertical stretch (lines in) (bits 10-0 only)
		set to one less than # lines in
81E4h	DWORD	K2 -- vertical stretch (stretch factor) (bits 10-0 only)
		set to -(#lines_in - #lines_out)

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81E8h	DWORD	DDA vertical accumulator (bits 11-0 only) (lines out) set to (#lines_out) - 1
81ECh	DWORD	streams FIFO and RAS control (see #M0067)
81F0h	DWORD	primary start coordinate (see #M0068)
81F4h	DWORD	primary window size (see #M0069)
81F8h	DWORD	secondary start coordinate (see #M0068)
81FCh	DWORD	secondary window size (see #M0069)

Note: changes to registers 81E0h-81E8h do not take effect until the next VSYNC

SeeAlso: #M0073,#M0057,#M0070

Bitfields for S3 Streams Processor primary stream control:

Bit(s)	Description	(Table M0059)
31	reserved	
30-28	filter characteristics	
	000	unchanged primary stream
	001	2X stretch by replicating pixels
	010	2X stretch by interpolating horizontally (replicating vertically)
		else reserved
27	reserved	
26-24	color mode	(see #M0060)
23-0	officially reserved,	but writing nonzero values can hang display

Notes: the primary stream is the output from the display RAM
bits 26-24 correspond to CR67 color mode field (see #P0688)

SeeAlso: #M0058,#M0061

(Table M0060)

Values for S3 Streams Processor color mode:

000b	eight bits per pixel
001b	YCrCb 4:2:2 unsigned, range 10h-F0h (secondary stream only)
010b	YUV 4:2:2, range 00h-FFh (secondary stream only)
011b	keyed high-color (1-5-5-5)
100b	YUV 2:1:1 two's complement (secondary stream only)
101b	high-color (5-6-5)
110b	reserved
111b	true-color (32bpp, high byte ignored)

SeeAlso: #M0059,#M0061

Bitfields for S3 Streams Processor secondary stream control:

Bit(s)	Description	(Table M0061)
31	reserved	
30-28	filter characteristics	
	000	unchanged secondary stream
	001	linear 0-2-4-2-0 for 1x-2x stretch
	010	bi-linear for 2x-4x stretch
	011	linear 1-2-2-2-1 for 4x+ stretch
		else reserved
28	enable smoothing between horizontally adjacent bits	(trial-and-error)

- 27 reserved
- 26-24 color mode (see #M0060,#M0074)
- 23-12 reserved
- 11-0 initial value of DDA horizontal accumulator
set to $2*(inwidth-1)-(outwidth-1)$

Notes: the secondary stream is typically live video, but can be pointed at any part of video memory
changes to this register do not take effect until the next VSYNC

SeeAlso: #M0058,#M0059,#M0062

Bitfields for S3 Streams Processor stretch/filter constants:

- | Bit(s) | Description | (Table M0062) |
|--------|---|---------------|
| 31-27 | reserved | |
| 26-16 | K2 horizontal scaling factor (input width - output width) | |
| 15-11 | reserved | |
| 10-0 | K1 horizontal scaling factor (input width - 1) | |

Note: changes to this register do not take effect until the next VSYNC

SeeAlso: #M0061

Bitfields for S3 Streams Processor chroma-key control:

- | Bit(s) | Description | (Table M0063) |
|--------|---|---------------|
| 31-29 | reserved | |
| 28 | key control | |
| | =1 normal color-key or chroma-key | |
| | =0 (keyed RGB 1-5-5-5 mode only) extract key from high bit of input stream; if key bit is clear, show pixel from other stream | |
| 27 | reserved | |
| 26-24 | color comparison precision | |
| | 000 compare bit 7 of R,G, and B values only | |
| | 001 compare bits 7-6 | |
| | ... | |
| | 111 compare bits 7-0 | |
| 23-0 | chroma-key color value | |
| | 23-16 = red or Y | |
| | 15-8 = green or U/Cb | |
| | 7-0 = blue or V/Cr | |

Note: if the keyed stream is YUV or YCrCb, then this register contains the lower bound and 8194h contains the upper bound of the chromakey value

SeeAlso: #M0058

Bitfields for S3 Streams Processor blend control:

- | Bit(s) | Description | (Table M0064) |
|--------|---|---------------|
| 31-27 | reserved (unused) | |
| 26-24 | blend type | |
| | 000 show secondary stream (video) overlaying primary stream | |
| | 001 show primary stream overlaying secondary stream | |
| | 010 blend pri/sec. streams (dissolve, secondary intensity = full-prim.) | |

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- 011 blend pri/sec. streams
 - 100 reserved (blank display)
 - 101 show secondary stream only where chroma-key color present
 - 110 show secondary stream (video) unconditionally
 - 111 reserved (blank display)
 - 23-14 reserved
 - 13 ??? (officially reserved, but set by S3_32.DLL)
 - 12-8 primary stream intensity (00h-1Ch, must be multiple of 4)
 - 4-0 secondary stream intensity (00h-1Ch, must be multiple of 4)
(ignored for blend type 010)
- Notes: for blend type 011, the primary and secondary stream intensities should not total more than 20h to avoid wraparounds which appear as incorrect colors; for blend type 010, the secondary stream intensity is automatically computed as 20h - bits12-8
changes to this register do not take effect until the next VSYNC
- SeeAlso: #M0058

Bitfields for S3 Streams Processor double-buffer/LPB control:

- | Bit(s) | Description | (Table M0065) |
|--------|--|---------------|
| 31-7 | reserved (unused; all but bit 7 appear to be read-only, as well) | |
| 6 | LPB frame buffer auto-toggle | |
| | if set, End-of-Frame toggles bit 4 | |
| 5 | delay loading LPB input buffer select until next End-of-Frame | |
| 4 | LPB input buffer select (see #M0073) | |
| | 0 use LPB frame buffer address 0 (FF0Ch) for incoming video data | |
| | 1 use LPB frame buffer address 1 (FF10h) | |
| 3 | reserved | |
| 2-1 | secondary stream buffer select | |
| | 00 use frame buffer address 0 (81D0h) | |
| | 01 use frame buffer address 1 (81D4h) | |
| | 1x use frame buffer 0/1 (81D0h/81D4h) selected by bit 4 for secondary stream and selected LPB frame buffer for LPB input | |
| 0 | primary stream buffer select | |
| | =0 use frame buffer address 0 (81C0h) | |
| | =1 use frame buffer address 1 (81C4h) | |

SeeAlso: #M0058,#M0073

Bitfields for S3 Streams Processor opaque overlay control:

- | Bit(s) | Description | (Table M0066) |
|--------|---|---------------|
| 31 | enable opaque overlay control | |
| 30 | select top stream (0 = secondary on top, 1 = primary) | |
| 29 | reserved | |
| 28-19 | pixel resume fetch | |
| | number of quadwords from background's left edge to position at which to start fetching pixels again | |
| 18-13 | reserved | |
| 12-3 | pixel stop fetch | |
| | number of quadwords from background's left edge to position at which | |

to stop fetching pixels

2-0 reserved

SeeAlso: #M0058

Bitfields for S3 Streams Processor streams FIFO and RAS control register:

Bit(s)	Description (Table M0067)
31-22	reserved (0)
21	skip 0.5 MCLK delay of PD[63:0] output (default = 0)
20	skip memory arbitration for ROM cycles (default = 0)
19	do not tristate PD[63:16] during ROM cycles (default = 0) (set by Win95 driver when using ISA bus)
18	EDO wait state control (LPB memory cycles only) =0 two-cycle accesses =1 one-cycle EDO accesses
17	reserved
16	RAS# pre-charge control =0 use CR68(bit3) setting (2.5/3.5 MCLKs) =1 1.5 MCLKs
15	RAS# low control =0 use CR68(bit2) setting (3.5/4.5 MCLKs) =1 2.5 MCLKs
14-10	primary stream FIFO threshold number of filled quadword slots at which to request refilling
9-5	secondary stream FIFO threshold number of filled quadword slots at which to request refilling
4-0	FIFO allocation, in quadword slots 00000 primary stream = 24, secondary = 0 01000 primary stream = 16, secondary = 8 01100 primary stream = 12, secondary = 12 10000 primary stream = 8, secondary = 16 11000 primary stream = 0, secondary = 24 else reserved

SeeAlso: #M0058

Bitfields for S3 Streams Processor start coordinate:

Bit(s)	Description (Table M0068)
31-27	reserved (read-only)
26-16	X coordinate (column) of upper left corner, plus 1
15-11	reserved (read-only)
10-0	Y coordinate (row) of upper left corner, plus 1

SeeAlso: #M0058,#M0069

Bitfields for S3 Streams Processor window size:

Bit(s)	Description (Table M0069)
31-27	reserved (read-only)
26-16	width in pixels - 1
15-11	reserved (read-only)
10-0	height in scan lines

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SeeAlso: #M0058,#M0068

-----V-MA0008200-----

MEM A000h:8200h - S3 VIRGE - MEMORY-MAPPED MEMORY-PORT CONTROL REGISTERS

Size: 40 BYTES

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

Format of S3 memory-maped port control registers:

Offset Size Description (Table M0070)

8200h DWORD FIFO control

8204h DWORD MIU control

8208h DWORD streams timeout

820Ch DWORD miscellaneous timeout

8210h 4 DWORDs ???

8220h DWORD DMA read base address

8224h DWORD DMA read stride width

SeeAlso: #M0057

-----V-MA00082E8-----

MEM A000h:82E8h - S3 - MEMORY-MAPPED CURRENT Y POSITION REGISTER

Size: WORD

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

SeeAlso: PORT 82E8h

-----V-MA00083B0-----

MEM A000h:83B0h - S3 - MEMORY-MAPPED VGA REGISTERS

Size: 48 BYTES

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

SeeAlso: PORT 03B0h,PORT 03C0h,PORT 03D0h

-----V-MA0008504-----

MEM A000h:8504h - S3 ViRGE - MEMORY-MAPPED SUBSYSTEM REGISTERS

Size: 12 BYTES

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

Format of S3 memory-mapped subsystem registers:

Offset Size Description (Table M0071)

8504h DWORD subsystem Control/Status Register (see PORT 42E8h,PORT 9AE8h)
on read:

bit 13 indicates whether graphics processor is busy

bits 12-8 indicate number of free FIFO slots

8508h DWORD ???

850Ch DWORD advanced function control (see PORT 4AE8h)

SeeAlso: #M0073,#M0057,#M0072

-----V-MA0008580-----

MEM A000h:8580h - S3 - MEMORY-MAPPED DMA REGISTERS

Size: 32 BYTES

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

Format of S3 memory-mapped DMA registers:

Offset	Size	Description	(Table M0072)
8580h	DWORD	start address in system memory	
8584h	DWORD	transfer length	
8588h	DWORD	transfer enable	
858Ch	DWORD	???	
8590h	DWORD	DMA base address	
8594h	DWORD	DMA write pointer	
8598h	DWORD	DMA read pointer	
859Ch	DWORD	DMA enable	

SeeAlso: #M0057,#M0073

-----V-MA00086E8-----

MEM A000h:86E8h - S3 - MEMORY-MAPPED ENHANCED REGISTERS

Size: ? BYTES

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

-----V-MA000A000-----

MEM A000h:A000h - S3 - MEMORY-MAPPED COLOR PALETTE REGISTERS

Size: 448 BYTES

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

-----V-MA000A4D4-----

MEM A000h:A4D4h - S3 - MEMORY-MAPPED BLT-FILL REGISTERS

Size: 60 BYTES

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

A4D4h	DWORD	???
A4D8h	DWORD	???
A4DCh	DWORD	??? (set to 07FFh by S3_32.DLL)
A4E0h	DWORD	??? (set to 07FFh by S3_32.DLL)
A4E4h	DWORD	???
A4E8h	DWORD	???
A4ECh	DWORD	???
A4F0h		
A4F4h	DWORD	???
A4F8h		
A4FCh	DWORD	???

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A500h DWORD ???
A504h DWORD ???
A508h DWORD ???
A50Ch DWORD ???

-----V-MA000A8D4-----

MEM A000h:A8D4h - S3 - MEMORY-MAPPED LINE REGISTERS

Size: 172 BYTES

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

-----V-MA000ACD4-----

MEM A000h:ACD4h - S3 - MEMORY-MAPPED POLYGON-FILL REGISTERS

Size: 172 BYTES

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

-----V-MA000B0D4-----

MEM A000h:B0D4h - S3 - MEMORY-MAPPED 3D-LINE REGISTERS

Size: 172 BYTES

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

-----V-MA000B4D4-----

MEM A000h:B4D4h - S3 - MEMORY-MAPPED 3D-TRIANGLE REGISTERS

Size: 172 BYTES

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

-----V-MA000FF00-----

MEM A000h:FF00h - S3 - MEM-MAPPED "SCENIC HIGHWAY" (Local Periph. Bus) ACCESS

Size: 64 DWORDS

Note: the S3 graphics processor registers can be mapped at either linear 000A0000h or at offset 16M from the start of the linear frame buffer

SeeAlso: MEM A000h:8180h

Format of S3 Local Peripheral Bus memory-mapped registers:

Offset Size Description (Table M0073)

FF00h DWORD LPB mode (see #M0074)

FF04h DWORD LPB FIFO status (see #M0075)

FF08h DWORD interrupt status (see #M0076)

FF0Ch DWORD frame buffer address 0 (bits 21-0, multiple of 8)
offset within frame buffer at which to store incoming data from LPB when Streams Processor double-buffer control (see #M0065) bit 4 clear

FF10h DWORD frame buffer address 1 (bits 21-0, multiple of 8)
offset within frame buffer at which to store incoming data from LPB when Streams Processor double-buffer control (see #M0065)

bit 4 is set

FF14h DWORD "direct address" = index for FF18h (see #M0077)

FF18h DWORD "direct data" (see #M0077)

Note: the direct address/direct data registers presumably rely on the attached device inserting data into the digital video stream, as on a Diamond Stealth64 Video, the "direct data" appears to reflect the video stream data (i.e. it varies, but with a pattern that depends on the video image, and stops varying when video is frozen)

FF1Ch DWORD general purpose I/O (see #M0078)

FF20h DWORD LPB serial port -- I2C/DDC access (see #M0079)

FF24h DWORD input window size (high word = rows, low word = columns)

FF28h DWORD data offsets
(video alignment; high word = rows ; low word = columns)

FF2Ch DWORD horizontal decimation
bits 0-31 set indicate that bytes 0-31 (mod 32) of each line should be dropped (in Video16 mode, each bit controls a WORD); decimation is aligned with the start of line as specified by the data offsets at FF28h

FF30h DWORD vertical decimation
bits 0-31 set indicate that lines 0-31 (mod 32) should be dropped, i.e. setting this DWORD to 55555555h will drop every other line; decimation starts with VSYNC regardless of the data offsets specified at FF28h

FF34h DWORD line stride (number of bytes between starts of successive lines of video data)
must be multiple of 4 -- lowest two bits forced to 0

FF38h 3 DWORDs unused??? (seem to echo FF34h)

FF40h 8 DWORDs LPB output FIFO - data transfer
writing to ANY of these DWORDs transfers a value to the FIFO; this organization allows use of a REP MOVSD instruction to fill the FIFO
on ISA bus, there must be a delay between successive writes

SeeAlso: #M0058

Bitfields for S3 Local Peripheral Bus LPB Mode register:

Bit(s)	Description	(Table M0074)
0	enable LPB	
3-1	LPB operational mode	
	000 Scenic/MX2	
	001 Video 16 (PCI only)	
	010 Video 8 In	
	used by Philips SAA7110/SAA7111 and Diamond's DTV1100	
	011 Video 8 In/Out	
	used by CL-480	
	100 Pass-Through	
	send FIFO data written by CPU through the decimation logic	
	else reserved (Trio64V+)	

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- 4 LBP Reset
pulse this bit before changing operational mode
- 5 skip every other frame
=0 write all received frames to memory
- 6 disable byte-swapping
=0 incoming 8-bit video is in order U, Y0, V, Y1 (CL-480)
=1 incoming 8-bit video is in order Y0, U, Y1, V (SAA711x)
(refer to bit 26 below)
- 8-7 officially reserved
- 7 ??? messes up video image when set
- 9 LPB vertical sync input polarity
=0 active low
=1 active high
- 10 LPB horizontal sync input polarity
=0 active low
=1 active high
- 11 (write-only) CPU VSYNC
writing a 1 makes Trio act as if LPB VSYNC had been received
- 12 (write-only) CPU HSYNC
writing a 1 makes Trio act as if LPB HSYNC had been received
- 13 (write-only) load base address
writing a 1 causes an immediate load of the currently active base address
- 15-14 reserved
- 17-16 maximum compressed data burst, LPB to Scenic/MX2
00 one DWORD
01 two DWORDs
10 three DWORDs
11 burst until empty (must ensure that MX2's 8-entry FIFO is not overrun)
- 20-18 reserved
- 22-21 video FIFO threshold
number of filled slots at which to request that Trio's memory manager begin to empty the FIFO (00 = one slot, 01 = two slots, 10 = four slots, 11 = six slots)
- 23 reserved (read-only)
- 24 LPB clock source
=0 driven by SCLK (Pin194) (for Trio64-compatibility mode)
=1 driven by LCLK (Pin148) (default)
- 25 don't add line stride after first HSYNC within VSYNC
must be set if first HSYNC occurs before VSYNC goes active
- 26 invert LCLK (only has effect if bit 24 set)
- 27 reserved
- 28 (not yet on Trio64V+) current odd/even video field status
- 29 (not yet on Trio64V+) field inversion - when set, the LPB's FIELD pin state is inverted before being reported in bit 28
- 30 reserved
- 31 (read-only) current state of CFLEVEL input (Pin182) in Video In/Out

mode (refer to bits 3-1)

SeeAlso: #M0073

Bitfields for S3 Local Peripheral Bus LPB FIFO status:

Bit(s)	Description	(Table M0075)
31	video FIFO 1 is almost empty (has exactly one full slot)	
30	video FIFO 1 is empty	
29	video FIFO 1 is full	
28-23	reserved	
22	video FIFO 0 is almost empty (has exactly one full slot)	
21	video FIFO 0 is empty	
20	video FIFO 0 is full	
19-14	reserved	
13	output FIFO is almost empty (has exactly one full slot)	
12	output FIFO is empty	
11	output FIFO is full	
10-4	reserved	
3-0	number of free four-byte slots in FIFO (there are 8 slots)	

SeeAlso: #M0073,#M0076

Bitfields for S3 Local Peripheral Bus interrupt status:

Bit(s)	Description	(Table M0076)
31-25	reserved	
24	drive serial port clock line low on receipt of start condition (causes I2C wait states until interrupt handler responds to start cond)	
23-20	reserved	
19	enable interrupt on I2C start condition detection	
18	enable interrupt on end of frame (VSYNC received)	
17	enable interrupt on end of line (HSYNC received)	
16	enable interrupt on LPB output FIFO empty	
15-4	reserved	
3	serial port detected I2C start condition	
2	VSYNC received (end of frame)	
1	HSYNC received (end of line)	
0	LPB output FIFO emptied	

Note: bits 3-0 are write-clear: writing a 1 to a bit resets it

SeeAlso: #M0073,#P0721

(Table M0077)

Values for S3 Local Peripheral Bus "direct address" index:

0000h	CP3 installation (FF18h reads 00C3h if installed)
0001h	?
0002h	?
0003h	?
	bit 7: ???
	bits 6-0: ???
0004h	?
0005h	?

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bits 7-0: ???

0020h ? (set to 107D4h, 1xD4h by CP3.DLL)

0028h ?

0034h ? (set to 10000h by CP3.DLL)

0414h ? (set by CP3.DLL)

0500h ?

0504h ?

0508h ?

050Ch ?

0510h ?

SeeAlso: #M0073

Bitfields for S3 Local Peripheral Bus General-Purpose I/O:

Bit(s) Description (Table M0078)

3-0 values to drive onto LPB GP output lines whenever CR5C is written

7-4 values of GP input lines (read-only), latched whenever CR5C is read

31-8 unused (read-only 0)

SeeAlso: #M0073

Bitfields for S3 Local Peripheral Bus serial-port register:

Bit(s) Description (Table M0079)

0 I2C clock line [SCL] (write)

=1 tri-state SCL, allowing other devices to pull it low

1 I2C data line [SDA] (write)

=1 tri-state SDA, allowing other devices to pull it low

2 I2C clock line (read)

this bit reflect the actual state of the SCL line

3 I2C data line (read)

this bit reflect the actual state of the SDA line

4 enable I2C interface

=0 disable bits 0/1, forcing both SCL and SDA to be tri-stated

15-5 reserved (unused)

20-16 mirrors of bits 4-0

(these bits are on the data bus' byte lane 2 to make them accessible via I/O port 00E2h)

Notes: see file I2C.LST for details of the I2C device registers accessible through this interface (VPX3220A for Stealth64 Video 2001TV) when the feature connector is disabled on the Stealth64 Video, these bits are connected to the monitor's DDC data and clock lines the official documentation erroneously lists the mirrors in bits 12-8 instead of 20-16

SeeAlso: #M0073,PORT 00E2h,#P0677

-----V-MB0000000-----

MEM B000h:0000h - MDA TEXT BUFFER

Size: 4096 BYTES

-----V-MB0000000-----

MEM B000h:0000h - HGC+ RAMFont-MODE TEXT BUFFER

Size: 16384 BYTES

Note: in RAMFont Mode 1, the memory is filled with the usual character/attribute pairs; in RAMFont Mode 2, four bits of each 'attribute' byte is used to provide 12 bits for specifying the character

-----V-MB0000000-----

MEM B000h:0000h - HGC GRAPHICS BUFFER (PAGE 0)

Size: 32768 BYTES

-----V-MB4000000-----

MEM B400h:0000h - HGC+ RAMFont BUFFER

Size: 4096 BYTES

Notes: apparently write-only

RAMFont Mode 1: 256 characters (8 bits each for char and attribute)

RAMFont Mode 2: 3072 characters (12 bits for char, 4 bits for attrib)

each character definition is 8 pixels wide (with 9th-column duplication if appropriate) by 8-16 pixels high

-----V-MB8000000-----

MEM B800h:0000h - CGA TEXT/GRAPHICS BUFFER

Size: 16384 BYTES

-----V-MB8000000-----

MEM B800h:0000h - EGA/VGA+ TEXT BUFFER

Size: 32768 BYTES

-----V-MB8000000-----

MEM B800h:0000h - HGC GRAPHICS BUFFER (PAGE 1)

Size: 32768 BYTES

-----V-MBFF00000-----

MEM BFF0h:0000h - ET4000/W32 ACL accelerator

Size: 169 BYTES

Format of ET4000/W32 memory-mapped registers:

Offset Size Description (Table M0080)

00h	DWORD	MMU Registers: memory base pointer register 0 (see #M0081)
04h	DWORD	MMU Registers: memory base pointer register 1 (see #M0081)
08h	DWORD	MMU Registers: memory base pointer register 2 (see #M0081)
0Ch	7 BYTES	???
13h	BYTE	MMU Registers: MMU control register (see #M0082)
14h	28 BYTES	???
30h	BYTE	Non-Queued Registers: suspend/terminate
31h	BYTE	Non-Queued Registers: operation state (see #M0083) (write-only)
32h	BYTE	Non-Queued Registers: sync enable
33h	BYTE	???
34h	BYTE	Non-Queued Registers: interrupt mask
35h	BYTE	Non-Queued Registers: interrupt status
36h	BYTE	Non-Queued Registers: ACL status (read-only) bit 1: read status (RDST) 1=ACL active, queue not empty bit 0: write status (WRST) 1=queue full
37h	73 BYTES	???
80h	DWORD	Queued Registers: pattern address (see #M0084)
84h	DWORD	Queued Registers: source address (see #M0084)

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88h	WORD	Queued Registers: pattern Y offset (see #M0085)
8Ah	WORD	Queued Registers: source Y offset (see #M0085)
8Ch	WORD	Queued Registers: destination y offset (see #M0085)
8Eh	BYTE	Queued Registers: virtual bus size
8Fh	BYTE	Queued Registers: X/Y direction (see #M0086)
90h	BYTE	Queued Registers: pattern wrap (see #M0087)
91h	BYTE	???
92h	BYTE	Queued Registers: source wrap (see #M0087)
93h	BYTE	???
94h	WORD	Queued Registers: X position
96h	WORD	Queued Registers: Y position
98h	WORD	Queued Registers: X count (see #M0088)
9Ah	WORD	Queued Registers: Y count (see #M0088)
9Ch	BYTE	Queued Registers: routine control (see #M0089)
9Dh	BYTE	Queued Registers: reload control
9Eh	BYTE	Queued Registers: background ROP for mixing
9Fh	BYTE	Queued Registers: foreground ROP for mixing
A0h	DWORD	Queued Registers: destination address
A4h	DWORD	Queued Registers: internal pattern address
A8h	DWORD	Queued Registers: internal source address

Bitfields for ET4000/W32 memory base pointer register:

Bit(s)	Description	(Table M0081)
31-22	reserved	
21-0	memory base pointer	

SeeAlso: #M0080

Bitfields for ET4000/W32 MMU control register:

Bit(s)	Description	(Table M0082)
7	reserved	
6-4	linear address control (LAC)	
	bit 6: MMU aperture 2	
	bit 5: MMU aperture 1	
	bit 4: MMU aperture 0	
3	reserved	
t2-0	aperture type (APT)	
	bit 2: MMU aperture 2	
	bit 1: MMU aperture 1	
	bit 0: MMU aperture 0	

SeeAlso: #M0080

Bitfields for ET4000/W32 operation state register:

Bit(s)	Description	(Table M0083)
7-4	reserved	
3	restart operation after ACL-interruption	
2-1	reserved	
0	restore status before ACL-interruption	

SeeAlso: #M0080

Bitfields for ET4000/W32 memory address register:

Bit(s) Description (Table M0084)

31-22 reserved

21-0 memory base pointer

SeeAlso: #M0080

Bitfields for ET4000/W32 offset register:

Bit(s) Description (Table M0085)

15-12 reserved

11-0 Y offset

SeeAlso: #M0080

Bitfields for ET4000/W32 X/Y direction register:

Bit(s) Description (Table M0086)

7-2 reserved

1 X direction

0 Y direction

SeeAlso: #M0080

Bitfields for ET4000/W32 wrap register:

Bit(s) Description (Table M0087)

7 reserved

6-4 pattern Y wrap

000 = 1 line

001 = 2 lines

010 = 4 lines

011 = 8 lines

100 = reserved

101 = reserved

110 = reserved

111 = no wrap

3 reserved

2-0 pattern X wrap

000 = reserved

001 = reserved

010 = 4 byte

011 = 8 byte

100 = 16 byte

101 = 32 byte

110 = 64 byte

111 = no wrap

SeeAlso: #M0080

Bitfields for ET4000/W32 count register:

Bit(s) Description (Table M0088)

15-12 reserved

11-0 pixel count

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SeeAlso: #M0080

Bitfields for ET4000/W32 routine control register:

Bit(s) Description (Table M0089)

7-6 reserved

5-4 routing of CPU address (ADRO)
00 don't use CPU address
01 CPU address is destination
10 reserved
11 reserved

3 reserved

2-0 routing of CPU data (DARQ)
000 don't use CPU data
001 CPU data is source data
010 CPU data is mixed data
011 reserved
100 CPU data is x-count
101 CPU data is y-count
10x reserved

SeeAlso: #M0080

-----V-MC0000000-----

MEM C000h:0000h - VIDEO BIOS (EGA and newer)

Size: varies (usually 16K-24K for EGA, 24K-32K for VGA)

-----b-MC0000000-----

MEM C000h:0000h OLIVETTI 640x400 GRAPHICS CARDS

Size: 62 BYTES

SeeAlso: MEM 0040h:0088h"Olivetti"

Format of Olivetti 640x480 ROM signatures:

Offset Size Description (Table M0133)

00h WORD 55AAh adapter ROM signature (check this!)

...

10h 2 BYTES "OL" if Olivetti EGA or VGA card

...

22h 2 BYTES (Olivetti EGA/VGA)

"VG" for Olivetti VGA (supports 640x400 mode)

"EG" for Olivetti EGA including Olivetti EGA card 2

...

3Ch 2 BYTES "PA" if Paradise card (supports 640x400 mode)

Note: These signatures can aid in the presence detection of an EGA or VGA adapter supporting the 640x400 mode.

Olivetti PC models M15 and M19 do not support the 640x400 mode (see INT 15h/C0h).

To decide if the 640x400 mode is supported by an Olivetti EGA card (only the Olivetti EGA card 2 supports it), also check that bit 7 and 5 are set at 0040h:0088h.

-----V-MC000xxxx-----

MEM C000h:xxxxh - VESA VBE v3.0 PROTECTED MODE INFORMATION BLOCK

Size: 20 BYTES

Range: starting at any byte within the first 32K of segment C000h

Format of VESA VBE 3.0 Protected Mode Information Block:

Offset	Size	Description (Table M0127)
00h	4 BYTES	signature "PMID"
04h	WORD	offset of protected-mode entry point within BIOS
06h	WORD	offset of protected-mode initialization entry point
08h	WORD	selector for BIOS data area emulation block (default 0000h, must be set by protected-mode OS to 16-bit read/write data selector with limit of at least 0600h)
0Ah	WORD	selector to access physical memory at A0000h (default A000h, must be set by protected-mode OS to 16-bit read/write data selector with 64K limit)
0Ch	WORD	selector to access physical memory at B0000h (default B000h, must be set by protected-mode OS to 16-bit read/write data selector with 64K limit)
0Eh	WORD	selector to access physical memory at B8000h (default B800h, must be set by protected-mode OS to 16-bit read/write data selector with 32K limit)
10h	BYTE	protected-mode execution (default 00h; set to 01h by OS when BIOS image is running in protected mode)
11h	BYTE	checksum byte for entire structure (this byte forces 8-bit sum of all bytes to 00h)

-----h-mC0000000-----

MEM C0000000h - Weitek "Abacus" math coprocessor

Size: 4096 BYTES

-----B-MC8000000-----

MEM C800h:0000h - HARD DISK BIOS

Size: varies (usually 8K or 16K)

-----V-MC8001C00-----

MEM C800h:1C00h - IBM XGA, XGA/A - MEMORY-MAPPED REGISTERS

Range: any 8K boundary within segments C000h to DFFFh

Notes: The XGA memory mapped registers can be assigned to the last 1K block in each 8K block in the range of C0000h-DFFFFh; the base offset of the 128 memory mapped location for a particular XGA instance is Segment: (1C00h+instance*80h) for each XGA installed in a system (default instance is 6). The instance number may be read from the XGA's Programmable Option Select registers

The XGA/A (PS/2 adapter) uses the 7KB area below the memory-mapped register area for ROM data; the XGA (PS/2 onboard) has included this area in its video BIOS ROM.

Most of the memory mapped registers are from the graphics coprocessor, while the I/O-registers are for the display controller.

-----V-MC0007FF8-----

MEM C000h:7FF8h - Matrox MGA Video Adapters - CARD VENDOR ID

Size: WORD

Desc: contains the PCI vendor ID for the card vendor; this is written into

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the video controllers PCI subsystem-vendor-ID field

SeeAlso: MEM C000h:7FFAh, MEM C000h:7FFCh

-----V-MC0007FFA-----

MEM C000h:7FFAh - Matrox MGA Video Adapters - HARDWARE REVISION ID

Size: BYTE

SeeAlso: MEM C000h:7FF8h, MEM C000h:7FFCh

-----V-MC0007FFC-----

MEM C000h:7FFCh - Matrox MGA Video Adapters - OFFSET OF PINS DATA STRUCTURE

Size: WORD

SeeAlso: INT 10/AX=4F14h"Matrox", #00126, MEM C000h:7FF8h

-----b-MF0000000-----

MEM F000h:0000h - WANG PC MEMORY MAPPED SCREEN BUFFER

Size: ???

Note: This is used by Peter Reilley's portable binary editor and viewer BEAV to directly write into the Wang PC's video screen buffer (instead of using INT 10/AH=02h,09h) after it has been mapped in by writing BYTE 01h to the screen port (PORT 1010h for the 1st screen, 1020h for the 2nd, 1030h for the 3rd, 1040h for the 4th). It will be unmapped afterwards by writing BYTE 00h to the screen port. Note, that this is only necessary when the INT 21/AX=4402h detection method resulted in non-IBM PC characteristic (return values other than 11h).

SeeAlso: MEM FC00h:3FC2h, INT 88h/AL=01h, INT 21h/4402h

-----B-MF0002DC5-----

MEM F000h:2DC5h - IBM AT SIGNATURE

Size: ??? signature

Note: Original IBM ATs with a multi-sector hard disk ROM-BIOS bug can be identified by checking a (currently unknown) signature at this location. This is known to be done by the Concurrent CP/M-86 family. Presumably the OS will then prohibit timer ISR dispatches within a code window of F000h:2D95h..F000h:2DD4h.

-----A-MF0006000-----

MEM F000h:6000h - IBM PC ROM BASIC

Size: 32768 BYTES

-----b-MF000800C-----

MEM F000h:800Ch ZENITH

Size: 8 BYTES signature "ZDS CORP"

Note: Zenith machines may have 256 Kb extra memory at 0FA0000h linear.

-----MF000C000-----

MEM F000h:C000h - Tandy ROM BIOS ID BYTE

Size: BYTE

Note: If the BYTE at this location is equal to 21h, some Microsoft software assumes this is a Tandy machine, and for example trusts the bits 1-0 at 0040h:00B5h.

SeeAlso: MEM 0040h:00B5h"Tandy", INT 15/AH=C0h

-----b-MFC000050-----

MEM FC00h:0050h - OLIVETTI Mxxx PC SIGNATURE

Size: 4 BYTES (or more) "OLIV"

Note: used by several Olivetti PCs, including M15, M19

SeeAlso: INT 15/AH=C0h

-----b-MFC003FC2-----

MEM FC00h:3FC2h - WANG PC SIGNATURE

Size: 4 BYTEs containing the signature "WANG"

Note: This is used by Peter Reilley's portable binary editor and viewer BEAV to detect a Wang PC.

SeeAlso: INT 88/AL=01h,INT 21/AX=4402h,INT 15/AH=C0h

-----B-MF000E000-----

MEM F000h:E000h - ORIGINAL IBM PC ROM BIOS

Size: 8192 BYTEs

-----b-MF000FFD9-----

MEM F000h:FFD9h - EISA MACHINE ID

Size: 4 BYTEs signature "EISA"

SeeAlso: INT 15/AH=E801h

-----b-MF000FFEO-----

MEM F000h:FFE0h - COMPAQ 386 MACHINES

Size: 16 BYTEs

SeeAlso: MEM 80C00000h

Format of Compaq 386 Memory Configuration Data:

Offset Size Description (Table M0134)

00h WORD Compaq 32-bit extra built-in memory available (FFFFh if not)

02h WORD Total size of Compaq extra memory

04h WORD Count of available paragraphs of Compaq extra memory

06h WORD Paragraph address of last paragraph in use as Compaq extra memory

08h 2 BYTEs product class signature "03"

0Ah 6 BYTEs signature "03COMPAQ"

Notes: The full "03COMPAQ" signature can be found in (at least) Compaq 386 machines which have dual harddisk controller. (see also CMOS 70h)

However, the 6-byte "COMPAQ" signature also seems to be available in other Compaq machines with dual hard disk controllers, at least the MS-DOS/PC DOS IO.SYS/IBMBIO.COM checks for it before it calls INT 15/AX=E400h and INT 15/AX=E480h.

Compaq's extra memory is mappable memory starting at FE00h:0000h growing downwards. It can be made available for example with Novell DOS 7+ EMM386.EXE /COMPAQ=ON.

Although this structure resides at a ROM-address it is actually write-protected RAM. To write to the structure to map in Compaq extra memory the write-protection must be temporarily disabled by setting bit 1 at WORD 80C00000h.

-----MF000FFE8-----

MEM F000h:FFE8h - Compaq - MACHINE SIGNATURE STRING

Size: 8 BYTEs

Desc: if this area contains the ASCII string "03COMPAQ", then this is a Compaq machine

SeeAlso: CMOS 1Bh"AMI"

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-----H-MF000FFFO-----

MEM F000h:FFF0h - RESET JUMP

Size: 5 BYTES

-----B-MF000FFF5-----

MEM F000h:FFF5h - ASCII BIOS DATE

Size: 8 BYTES

-----B-MF000FFFD-----

MEM F000h:FFFDh - OFTEN USED TO ENSURE CORRECT BIOS CHECKSUM

Size: BYTE

-----B-MF000FFFE-----

MEM F000h:FFFEh - MACHINE TYPE CODE

Size: BYTE

SeeAlso: INT 15/AH=C0h

-----X-MF000xxx0-----

MEM F000h:xxx0h - PCI IRQ Routing Table Specification v1.0

Size: N paragraphs (N >= 2)

InstallCheck: scan for the signature string "\$PIR" followed by a valid
PCI IRQ Routing Table

Range: any paragraph boundary within the range F0000h to FFFFh

Format of PCI IRQ Routing Table v1.0:

Offset	Size	Description	(Table M0090)
--------	------	-------------	---------------

00h	4 BYTES	signature "\$PIR"
-----	---------	-------------------

04h	WORD	version (0100h for v1.0)
-----	------	--------------------------

06h	WORD	table size in bytes
-----	------	---------------------

08h	BYTE	bus number for PCI Interrupt Router
-----	------	-------------------------------------

09h	BYTE	device/function number for PCI Interrupt Router
-----	------	---

0Ah	WORD	bitmap of PCI-exclusive IRQs (bit 0 = IRQ0, etc.)
-----	------	---

0Ch	WORD	PCI vendor ID for compatible PCI Interrupt Router
-----	------	---

0Eh	WORD	PCI device ID for compatible PCI Interrupt Router
-----	------	---

10h	DWORD	Miniport data
-----	-------	---------------

14h	11 BYTES	reserved (0)
-----	----------	--------------

1Fh	BYTE	checksum (set to make 8-bit sum of bytes in entire structure equal 00h)
-----	------	--

--- optional data ---

20h	16 BYTES	first slot entry (see #M0091)
-----	----------	-------------------------------

...

16 BYTES	Nth slot entry
----------	----------------

Format of PCI IRQ Routing Table slot entry:

Offset	Size	Description	(Table M0091)
--------	------	-------------	---------------

00h	BYTE	PCI bus number
-----	------	----------------

01h	BYTE	PCI device number (bits 7-3)
-----	------	------------------------------

02h	BYTE	link value for INTA#
-----	------	----------------------

03h	WORD	IRQ bitmap for INTA#
-----	------	----------------------

05h	BYTE	link value for INTB#
-----	------	----------------------

06h	WORD	IRQ bitmap for INTB#
-----	------	----------------------

08h	BYTE	link value for INTC#
-----	------	----------------------

- 09h WORD IRQ bitmap for INTC#
- 0Bh BYTE link value for INTD#
- 0Ch WORD IRQ bitmap for INTD#
- 0Eh BYTE slot number (00h = motherboard, other = vendor-specific)
- 0Fh BYTE reserved

SeeAlso: #M0090,#01260 at INT 1A/AX=B406h

-----B-MF000xxxx-----

MEM F000h:xxxxh - AWARD Flash Hook

Format of AWARD Flash BIOS interface:

- | Offset | Size | Description (Table M0092) |
|--------|---------|--|
| 00h | 8 BYTES | signature "AWDFLASH" |
| 08h | WORD | offset in F000h of FAR function: Get ???
Return: BL = ??? (00h) |
| 0Ah | WORD | offset in F000h of FAR function: ??? |
| 0Ch | WORD | offset in F000h of FAR function: ??? |
| 0Eh | WORD | offset in F000h of FAR function: ??? |
| 10h | WORD | offset in F000h of FAR function: ??? |
| 12h | WORD | offset in F000h of FAR function: Disable Shadowing |
| 14h | WORD | offset in F000h of FAR function: Enable Shadowing |
| 16h | WORD | offset in F000h of FAR function: Get ???
Return: DS:SI -> ??? (30 bytes?) |
| 18h | WORD | offset in F000h of FAR function: Set ???
DS:SI -> ??? (appears to be same as previous function) |

Note: the AWDFLASH utility copies the ROM from F000h and uses the copy instead of the original F000h:xxxxh addresses

-----B-MF000xxxx-----

MEM F000h:xxxxh - Asustek Flash Hook

Format of Asustek Flash interface:

- | Offset | Size | Description (Table M0093) |
|--------|----------|--|
| 00h | 10 BYTES | signature "ASUS_FLASH" |
| 0Ah | 6 BYTES | blanks (padding) |
| 10h | WORD | interface version??? (current PFLASH.EXE requires 0101h) |
| 12h | DWORD | -> position-independent code to enable shadowing |
| 16h | WORD | size of code pointed at by previous field (<= 0400h) |
| 18h | DWORD | -> position-independent code to disable shadowing |
| 1Ch | WORD | size of code pointed at by previous field (<= 0400h) |

-----p-Mxxxxxxx0-----

MEM xxxxh:xxx0h - Advanced Configuration and Power Interface Spec (ACPI) v0.9+

Range: any paragraph boundary in the first kilobyte of the XBDA, the last kilobyte of conventional memory, or from E000h:0000h to F000h:FFE0h

Note: scan paragraph boundaries for the signature string "RSD PTR ", followed by a valid Root System Description Pointer structure (see #M0094)

SeeAlso: INT 15/AX=E820h

!!!acpi\acpi10.pdf p.194

Format of ACPI Root System Description Pointer structure:

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Offset	Size	Description	(Table M0094)
00h	8 BYTES	signature "RSD PTR "	
08h	BYTE	checksum (entire structure, including this byte, must add up to zero)	
09h	6 BYTES	OEM identifier	
0Fh	BYTE	reserved (0)	
10h	DWORD	physical address of Root System Description Table (see #M0096)	

SeeAlso: #M0096

Format of ACPI System Description Table header:

Offset	Size	Description	(Table M0095)
00h	4 BYTES	signature	
04h	DWORD	length of table in bytes, including this header	
08h	BYTE	revision of specification corresponding to signature 01h for both v0.9 and v1.0	
09h	BYTE	checksum (set such that entire table sums to 00h)	
0Ah	6 BYTES	OEM identification	
10h	8 BYTES	OEM table identifier	
18h	4 BYTES	OEM revision number	

---ACPI v1.0---

1Ch	4 BYTES	vendor ID for table-creation utility used
20h	4 BYTES	revision of table-creation utility

SeeAlso: #M0094,#M0096,#M0099,#M0097,#M0100,#M0105,#M0108,#M0110

Format of ACPI Root System Description Table:

Offset	Size	Description	(Table M0096)
00h	36 BYTES	System Description Table Header (see #M0095) signature "RSDT"	
24h	N DWORDs	physical addresses of other description tables (see #M0099,#M0097,#M0100,#M0105,#M0108,#M0109)	

Notes: the number of table pointers is implied by the table length field in the header (at offset 04h)
for ACPI v0.9, the header is eight bytes smaller and thus all following offsets are 8 less

SeeAlso: #M0094

Format of ACPI Fixed ACPI Description Table:

Offset	Size	Description	(Table M0097)
00h	36 BYTES	System Description Table Header (see #M0095) signature "FACP"	
24h	DWORD	physical address of the Firmware ACPI Control Structure (see #M0105)	
28h	DWORD	physical address of the Differentiated System Description Table (see #M0099)	
2Ch	BYTE	interrupt mode 00h dual PIC (industry-standard AT-type) 01h multiple APIC (see #M0100) else reserved	

2Dh	BYTE	reserved
2Eh	WORD	system vector of SCI interrupt
30h	DWORD	I/O port address of SMI command port
34h	BYTE	value to write to SMI comamnd port to disable SMI ownership of ACPI hardware registers
35h	BYTE	value to write to SMI comamnd port to re-enable SMI ownership of ACPI hardware registers
36h	BYTE	(v1.0) value to write to SMI command port to enter S4BIOS state 00h if not supported
37h	BYTE	reserved
38h	DWORD	I/O port address of Power Management 1a Event Register Block
3Ch	DWORD	I/O port address of Power Management 1b Event Register Block (optional, 00000000h if not supported)
40h	DWORD	I/O port address of Power Management 1a Control Register Block
44h	DWORD	I/O port address of Power Management 1b Control Register Block (optional, 00000000h if not supported)
48h	DWORD	I/O port address of Power Management 2 Control Register Block (optional, 00000000h if not supported)
4Ch	DWORD	I/O port address of Power Management Timer Control Reg. Block
50h	DWORD	I/O port address of Generic Purpose Event 0 Register Block (optional, 00000000h if not supported)
54h	DWORD	I/O port address of Generic Purpose Event 1 Register Block (optional, 00000000h if not supported)
58h	BYTE	size of Power Management 1a/1b Event Register Block (≥ 4)
59h	BYTE	size of Power Management 1a/1b Control Register Block (≥ 1)
5Ah	BYTE	size of Power Management 2 Control Register Block (≥ 1)
5Bh	BYTE	size of Power Management Timer Control Register Block (≥ 4)
5Ch	BYTE	size of Generic Purpose Event 0 Register Block (multiple of 2)
5Dh	BYTE	size of Generic Purpose Event 1 Register Block (multiple of 2)
5Eh	BYTE	offset within General Purpose Event model for GPE1-based events
5Fh	BYTE	reserved
60h	WORD	worst-case hardware latency (microseconds) for entering/leaving state C2; >100 if C2 not supported
62h	WORD	worst-case hardware latency (microseconds) for entering/leaving state C3; >1000 if C3 not supported
64h	WORD	size of contiguous cacheable memory which must be read to flush all dirty lines from a processor's memory cache; use if fixed feature flag WBINVD (see #M0098) is clear 0000h if flushing not supported
66h	WORD	memory stride size (in bytes) to flush processor's memory cache
68h	BYTE	bit index of processor's duty cycle setting within the processor's P_CNT register
69h	BYTE	size of processor's duty cycle setting in bits
6Ah	BYTE	index within RTC CMOS RAM of the day-of-month alarm value 00h = not supported
6Bh	BYTE	index within RTC CMOS RAM of the month-of-year alarm value 00h = not supported
6Ch	BYTE	index within RTC CMOS RAM of the century alarm value

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00h = not supported

6Dh BYTE reserved

6Eh DWORD fixed feature flags (see #M0098)

SeeAlso: #M0094, CMOS 7Dh, CMOS 7Eh, CMOS 7Fh

Bitfields for ACPI Fixed Feature Flags:

Bit(s) Description (Table M0098)

0 WBINVD instruction is correctly supported by processor

1 WBINVD instruction flushes all caches and maintains coherency, but does not guarantee invalidation of all caches

2 all processors support C1 sleep state

3 C2 sleep state is configured to work on multiprocessor system

---v0.9---

4 power button is handled as a generic feature

5 RTC wake-up state is not supported in fixed register space

6 TMR_VAL size

=0 24 bits

=1 32 bits

7-31 reserved

---v1.0---

4 power button is handled as a control method device

5 =0 sleep button is handled as a fixed feature programming mode
=1 control method device, or no sleep button

6 RTC wake-up state is not supported in fixed register space

7 RTC alarm can wake system from S4 state

8 TMR_VAL size

=0 24 bits

=1 32 bits

9-31 reserved

SeeAlso: #M0097

Format of ACPI Differentiated System Description Table:

Offset Size Description (Table M0099)

00h 36 BYTES System Description Table Header (see #M0095)
signature "DSDT"

24h complex byte stream; refer to ACPI document and software

SeeAlso: #M0094

Format of ACPI Multiple APIC Description Table:

Offset Size Description (Table M0100)

00h 36 BYTES System Description Table Header (see #M0095)
signature "APIC"

24h DWORD physical address of the local APIC in each processor's address space

28h DWORD multiple-APIC flags (see #M0101)

2Ch 12N BYTES APIC structures (see #M0102, #M0104)

first byte of each is type, second is length; types other than 00h and 01h are currently reserved and should be skipped

SeeAlso: #M0094

Bitfields for ACPI Multiple APIC Description Table flags:

Bit(s)	Description	(Table M0101)
0	system contains AT-compatible dual 8259 interrupt controllers in addition to APICs	
1-31	reserved (0)	

SeeAlso: #M0100

Format of ACPI Local APIC Structure:

Offset	Size	Description	(Table M0102)
00h	BYTE	structure type (00h = Processor Local APIC)	
01h	BYTE	length of this structure (0Ch for v0.9, 08h for v1.0)	
02h	BYTE	processor ID	
03h	BYTE	processor's local APIC ID	

---v0.9---

04h	DWORD	physical address of APIC	
08h	DWORD	flags (TBD)	

--v1.0---

04h	DWORD	flags (see #M0103)	
-----	-------	--------------------	--

SeeAlso: #M0100,#M0104

Bitfields for ACPI Local APIC flags:

Bit(s)	Description	(Table M0103)
0	APIC enabled	
1-31	reserved (0)	

SeeAlso: #M0102

Format of ACPI I/O APIC Structure:

Offset	Size	Description	(Table M0104)
00h	BYTE	structure type (00h = Processor Local APIC)	
01h	BYTE	0Ch (length of this structure)	
02h	BYTE	I/O APIC's ID	
03h	BYTE	reserved (0)	
04h	DWORD	physical address of the APIC	
08h	DWORD	number of first system interrupt vector for APIC	

SeeAlso: #M0100,#M0102

Format of ACPI Firmware ACPI Control Structure:

Offset	Size	Description	(Table M0105)
00h	4 BYTES	signature "FACS"	
04h	DWORD	length of entire structure in bytes (>= 40h)	
08h	DWORD	value of system's hardware signature at last boot	
0Ch	DWORD	real-mode ACPI OS waking vector	
		if nonzero, control is transferred to this address on next BIOS POST	
10h	DWORD	global lock (see #M0107)	
14h	DWORD	(v1.0) firmware control structure flags (see #M0106)	

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18h 44 BYTES reserved (0)

Notes: this structure is located on a 64-byte boundary anywhere in the first 4GB of memory
the BIOS is required to omit the address space containing this structure from system memory in the system's memory map

SeeAlso: #M0094,INT 15/AX=E820h

Bitfields for ACPI Firmware Control Structure Feature flags:

Bit(s) Description (Table M0106)

0 system supports S4BIOS_REQ

=0 operating system must save/restore memory state in order to go to S4

1-31 reserved (0)

SeeAlso: #M0105

Bitfields for ACPI Embedded Controller Arbitration Structure:

Bit(s) Description (Table M0107)

0 request for Global Lock ownership is pending

1 Global Lock is currently owned

2-31 reserved

SeeAlso: #M0105

Format of ACPI Persistent System Description Table:

Offset Size Description (Table M0108)

00h 36 BYTES System Description Table Header (see #M0095)
signature "PSDT"

24h complex byte stream; refer to ACPI document and software

SeeAlso: #M0094

Format of ACPI Secondary System Description Table:

Offset Size Description (Table M0109)

00h 36 BYTES System Description Table Header (see #M0095)
signature "SSDT"

24h complex byte stream; refer to ACPI document and software

SeeAlso: #M0094

Format of ACPI Smart Battery Description Table:

Offset Size Description (Table M0110)

00h 36 BYTES System Description Table Header (see #M0095)
signature "SBST"

24h DWORD energy level in mWh at which system should warn user

28h DWORD energy level in mWh at which system should automatically enter
sleep state

2Ch DWORD energy level in mWh at which system should perform an emergency
shutdown

SeeAlso: #M0094

-----Mxxxxxxx0-----

MEM xxxxh:xxx0h - BIOS32 Service Directory

InstallCheck: scan paragraph boundaries E000h to FFFFh for signature string

"_32_", followed by a valid header structure (see #F0021)

SeeAlso: CALL xxxxh:xxxxh"BIOS32"

-----Mxxxxxxx0-----

MEM xxxxh:xxx0h - Desktop Management Interface / System Management BIOS

InstallCheck: scan paragraph boundaries F000h to FFFFh for signature string

"_DMI_", followed by a valid header structure (see #M0111,#M0112)

Format of Desktop Management Interface entry-point structure:

Offset	Size	Description	(Table M0111)
00h	5 BYTES	signature	"_DMI_"
05h	BYTE	checksum of this structure	(forces 8-bit sum of bytes to 00h)
06h	WORD	total length of SMBIOS structure table,	in bytes
08h	DWORD	32-bit physical address of read-only SMBIOS structure table	(see #F0059)
0Ch	WORD	number of SMBIOS structures	
0Eh	BYTE	BCD SMBIOS revision (high nybble = major, low = minor)	

!!!ftp://download.intel.com/ial/wfm/smbios.pdf

SeeAlso: #M0112

Format of System Management BIOS entry-point structure:

Offset	Size	Description	(Table M0112)
00h	4 BYTES	signature	"_SM_"
04h	BYTE	checksum of this structure	(forces 8-bit sum of bytes to 00h)
05h	BYTE	length of structure in bytes	(1Fh for v2.1+)
06h	BYTE	major version of specification	
07h	BYTE	minor version of specification	(01h = vX.1, 16h = vX.22)
08h	WORD	size of largest SMBIOS structure	(see also #F0046)
0Ah	BYTE	revision of this data structure	00h SMBIOS v2.1-2.3 01h-FFh reserved for future versions
0Bh	5 BYTES	revision-specific data	(currently unused)
10h	5 BYTES	intermediate anchor string	"_DMI_"
15h	BYTE	checksum of intermediate entry-point structure	(forces 8-bit sum of bytes 10h-1Eh to 00h)
16h	WORD	total length of SMBIOS structure table,	in bytes
18h	DWORD	32-bit physical address of read-only SMBIOS structure table	(see #F0059)
1Ch	WORD	number of SMBIOS structures	
1Eh	BYTE	BCD SMBIOS revision (high nybble = major, low = minor)	00h if specification version only given in bytes 06h/07h

BUG: due to an error in the v2.1 specification, some implementations might indicate a length of 1Eh bytes instead of 1Fh

SeeAlso: #M0111

-----Mxxxxxxx0-----

MEM xxxxh:xxx0h - Multiprocessor Specification - FLOATING POINTER STRUCTURE

InstallCheck: scan paragraph boundaries for the signature string "_MP_", followed by a valid floating pointer structure (see #M0113)

Range: any paragraph boundary in the first kilobyte of the XBDA, the last

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kilobyte of conventional memory, or from F000h:0000h to F000h:FFE0h

SeeAlso: MEM FEE00000h

Format of Multiprocessor Specification Floating Pointer structure:

Offset	Size	Description	(Table M0113)
00h	4 BYTES	signature "_MP_"	
04h	DWORD	physical address of MP configuration table (see #M0114)	
		00000000h if no configuration table	
08h	BYTE	length of this structure in paragraphs (currently 01h)	
09h	BYTE	revision of MP specification supported	
		01h = v1.1	
		04h = v1.4	
0Ah	BYTE	checksum (8-bit sum of entire structure, including this	
		byte, must equal 00h)	
0Bh	BYTE	MP feature byte 1: system configuration type	
		00h: MP configuration table present	
		nonzero: default configuration implemented by system	
0Ch	BYTE	MP feature byte 2	
		bit 7: IMCR present	
		bits 6-0: reserved (0)	
0Dh	3 BYTES	MP feature bytes 3-5 (reserved, must be 00h)	

Format of Multiprocessor Specification configuration table header:

Offset	Size	Description	(Table M0114)
00h	4 BYTES	signature "PCMP"	
04h	WORD	length of base configuration table in bytes, including	
		this header	
06h	BYTE	revision of MP specification supported	
		01h = v1.1	
		04h = v1.4	
07h	BYTE	checksum of entire base configuration table	
08h	8 BYTES	OEM identifier	
10h	12 BYTES	product ID	
1Ch	DWORD	physical address to OEM-defined configuration table	
		00000000h if not present	
20h	WORD	size of base OEM table in bytes (0000h if not present)	
22h	WORD	number of entries in variable portion of base table	
24h	DWORD	address of local APIC (see also MEM FEE0h:0020h)	
28h	WORD	length of extended entries following end of base table	
		(in bytes)	
2Ah	BYTE	checksum for extended table entries (includes only	
		extended entries following base table)	
2Ch	var	configuration table entries (see #M0115)	

SeeAlso: #M0113

Format of Multiprocessor Specification configuration table entries:

Offset	Size	Description	(Table M0115)
00h	BYTE	entry type code	

00h processor
 01h bus
 02h I/O APIC
 03h I/O interrupt assignment
 04h local interrupt assignment
 80h system address space mapping
 81h bus hierarchy descriptor
 82h compatibility bus address space modifier

---processor---

01h BYTE local APIC identifier
 02h BYTE local APIC version
 03h BYTE CPU flags
 bit 0: processor usable
 bit 1: bootstrap processor
 04h WORD CPU type
 bits 11-8: CPU family
 bits 7-4: CPU model
 bits 3-0: stepping
 (bits 11-0 all set indicate non-Intel-compatible CPU)
 06h 2 BYTES unused
 08h DWORD feature flags (as returned by Pentium CPUID instruction)
 0Ch 8 BYTES reserved

---bus---

01h BYTE bus ID (assigned sequentially from 00h by BIOS)
 02h 6 BYTES bus type (blank-padded ASCII string) (see #M0116)

---I/O APIC---

01h BYTE APIC identifier
 02h BYTE APIC version
 03h BYTE I/O APIC flags
 bit 0: enabled
 bits 7-1: reserved
 04h DWORD base address for APIC

---I/O,local interrupt assignment---

01h BYTE interrupt type
 00h vectored interrupt (from APIC)
 01h NMI
 02h system management interrupt
 03h vectored interrupt (from external PIC)
 02h BYTE APIC control (see #M0117)
 03h BYTE unused
 04h BYTE source bus identifier
 05h BYTE source bus IRQ
 06h BYTE destination I/O APIC identifier
 07h BYTE destination I/O APIC interrupt pin number

---system address space mapping---

01h BYTE entry length (14h)
 02h BYTE bus ID
 03h BYTE address type (00h I/O, 01h memory, 02h prefetch)

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04h	QWORD	starting address of region visible to bus
0Ch	QWORD	length of region visible to bus
---bus hierarchy descriptor---		
01h	BYTE	entry length (08h)
02h	BYTE	bus ID
03h	BYTE	bus information bit 0: subtractive decoding
04h	BYTE	ID of parent bus
05h	3 BYTES	reserved
---compatibility bus address space modifier---		
01h	BYTE	entry length (08h)
02h	BYTE	bus ID
03h	BYTE	address modifier bit 0: remove address ranges in predefined range list from bus's address space
04h	DWORD	number indicating predefined address space range to be removed 00h ISA-compatible I/O range (x100h-x3FFh and aliases) 01h VGA-compatible I/O range (x3B0h-x3BBh,x3C0h-x3DFh,aliases)

SeeAlso: #M0114

(Table M0116)

Values for Multiprocessor Specification bus name:

"CBUS"	Corollary CBus
"CBUSII"	Corollary CBus II
"EISA"	
"FUTURE"	IEEE FutureBus
"INTERN"	internal bus
"ISA"	
"MBI"	Multibus I
"MBII"	Multibus II
"MCA"	Microchannel
"MPI"	
"MPSA"	
"NUBUS"	Apple Macintosh NuBus
"PCI"	
"PCMCIA"	
"TC"	DEC TurboChannel
"VL"	VESA Local Bus
"VME"	VMEbus
"XPRESS"	Express System Bus

SeeAlso: #M0115

Bitfields for Multiprocessor Specification APIC control:

Bit(s)	Description	(Table M0117)
1-0	input signal polarity	
	00	conforms to bus specification
	01	active high
	10	reserved

- 11 active low
- 3-2 trigger mode
 - 00 conforms to bus specification
 - 01 edge-triggered
 - 10 reserved
 - 11 level-triggered

SeeAlso: #M0115

-----H-mFEC00000-----

MEM FEC00000h - Pentium - 82379AB I/O APIC - I/O REGISTER SELECT

Size: DWORD

Desc: bits 7-0 of the I/O Register Select memory location specify which of the APIC's registers appears in the I/O Window at FE_{xx}010h

Range: the Multiprocessor Specification calls for I/O APICs to be memory-mapped on 4K boundaries between FEC00000h and FEDFC000h; the Intel 82379AB I/O APIC can be memory-mapped on any 1K boundary within FEC0000h-FEC0F800h

Note: this memory-mapped register is also supported by the Intel 82093AA I/O APIC

SeeAlso: MEM FEC00010h, MEM FEE00000h, MEM _{xxxxh}:_{xxx0h}"Multiprocessor"

-----H-mFEC00010-----

MEM FEC00010h - Pentium - 82379AB I/O APIC - I/O WINDOW

Size: DWORD

Range: the Multiprocessor Specification calls for I/O APICs to be memory-mapped on 4K boundaries between FEC00000h and FEDFC000h

Note: this memory-mapped register is also supported by the Intel 82093AA I/O APIC

SeeAlso: MEM FEC00010h

(Table M0118)

Values for Intel 82379AB/82093AA I/O APIC registers:

- 00h APIC ID
- 01h APIC version (read-only)
 - bits 31-24: reserved
 - bits 23-16: maximum redirection entry
 - bits 15-8: reserved
 - bits 7-0: APIC version (11h for 82093AA)
- 02h APIC arbitration ID (read-only)
 - bits 31-28: reserved
 - bits 27-24: arbitration ID
 - bits 23-0: reserved
- 10h-11h redirection table entry 0 (10h=low DWORD, 11h=high DWORD)
- 12h-13h redirection table entry 1 (see !!!)
- ...
- 2Eh-2Fh redirection table entry 15
- 82093AA only---
- 30h-31h redirection table entry 16
- ...
- 3Eh-3Fh redirection table entry 23

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Bitfields for APIC redirection table entry:

Bit(s) Description (Table M0119)

63-56 destination

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55-17 reserved

16 interrupt mask

15 trigger mode

14 remote IRR (read-only)

13 interrupt input pin polarity

12 delivery status (read-only)

11 destination mode

10-8 delivery mode

7-0 interrupt vector (10h-FEh)

-----H-mFEE00000-----

MEM FEE00000h - Pentium - LOCAL APIC

Size: 4096 BYTEs

Notes: the Advanced Programmable Interrupt Controller built into multiprocessor-capable Pentiums (P54C, etc. -- basically 75MHz and faster Pentiums) maps its registers into the top of the physical address space on data reads and writes, but not on code reads; data accesses to the APIC registers do not cause external bus cycles

the APIC's registers are only visible when the APIC is enabled (which occurs at CPU reset when external data lines contain proper signals); all accesses to APIC registers should use 32-bit reads or writes, as 8-bit and 16-bit accesses may produce unpredictable results the PentiumPro (P6) permits the address at which the local APIC appears to be changed with Model-Specific Register 0000001Bh

SeeAlso: MEM FEC00000h, MEM FEE00020h, MEM xxxxh:xxx0h"Multiprocessor"

SeeAlso: MSR 0000001Bh

-----H-mFEE00020-----

MEM FEE00020h - Pentium - LOCAL APIC - LOCAL APIC ID REGISTER

Size: DWORD

SeeAlso: MEM FEE00030h

-----H-mFEE00030-----

MEM FEE00030h - Pentium - LOCAL APIC - LOCAL APIC VERSION REGISTER

Size: DWORD

Note: read-only

SeeAlso: MEM FEE00020h

-----H-mFEE00040-----

MEM FEE00040h - Pentium - LOCAL APIC - RESERVED

SeeAlso: MEM FEE00000h

-----H-mFEE00050-----

MEM FEE00050h - Pentium - LOCAL APIC - RESERVED

SeeAlso: MEM FEE00000h

-----H-mFEE00060-----

MEM FEE00060h - Pentium - LOCAL APIC - RESERVED

SeeAlso: MEM FEE00000h

-----H-mFEE00070-----

MEM FEE00070h - Pentium - LOCAL APIC - RESERVED

SeeAlso: MEM FEE00000h

-----H-mFEE00080-----

MEM FEE00080h - Pentium - LOCAL APIC - TASK PRIORITY REGISTER (TPR)

Size: DWORD

-----H-mFEE00090-----

MEM FEE00090h - Pentium - LOCAL APIC - ARBITRATION PRIORITY REGISTER (APR)

Size: DWORD

Note: read-only

-----H-mFEE000A0-----

MEM FEE000A0h - Pentium - LOCAL APIC - END OF INTERRUPT REGISTER (EOI)

Size: DWORD

Note: write-only

-----H-mFEE000A0-----

MEM FEE000A0h - Pentium - LOCAL APIC - PROCESSOR PRIORITY REGISTER (PPR)

Size: DWORD

Note: read-only

SeeAlso: MEM FEE00000h

-----H-mFEE000B0-----

MEM FEE000B0h - Pentium - LOCAL APIC - RESERVED

SeeAlso: MEM FEE00000h

-----H-mFEE000C0-----

MEM FEE000C0h - Pentium - LOCAL APIC - REMOTE READ REGISTER

Size: DWORD

Note: read-only

-----H-mFEE000D0-----

MEM FEE000D0h - Pentium - LOCAL APIC - LOGICAL DURATION REGISTER (LDR)

Size: DWORD

SeeAlso: MEM FEE00000h

-----H-mFEE000E0-----

MEM FEE000E0h - Pentium - LOCAL APIC - DESTINATION FORMAT REGISTER (DFR)

Size: DWORD

bits 27-0: read-only

bits 31-28: read-write

-----H-mFEE000F0-----

MEM FEE000F0h - Pentium + - LOCAL APIC - SPURIOUS INTERRUPT VECTOR REGISTER

Size: DWORD

Bitfields for Local APIC Spurious Interrupt Vector register:

Bit(s) Description (Table M0126)

63-10 reserved

9 disable focus processor checking during lowest-priority delivery

8 APIC enabled by software

7-4 spurious vector number

3-0 reserved (1)

-----H-mFEE00100-----

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MEM FEE00100h - Pentium + - LOCAL APIC - IN-SERVICE REGISTER (ISR)

Size: 128 BYTES

Note: read-only

SeeAlso: MEM FEE00200h

-----H-mFEE00180-----

MEM FEE00180h - Pentium + - LOCAL APIC - TRIGGER MODE REGISTER (TMR)

Size: 128 BYTES

Note: read-only

SeeAlso: MEM FEE00000h

-----H-mFEE00200-----

MEM FEE00200h - Pentium + - LOCAL APIC - INTERRUPT REQUEST REGISTER (IRR)

Size: 128 BYTES

Note: read-only

SeeAlso: MEM FEE00100h

-----H-mFEE00280-----

MEM FEE00280h - Pentium + - LOCAL APIC - ERROR STATUS REGISTER

Size: DWORD

Note: read-only

Bitfields for Pentium APIC error status register:

Bit(s) Description (Table M0120)

0	send checksum error
1	receive checksum error
2	send accept error
3	receive accept error
4	reserved
5	send illegal vector
6	receive illegal vector
7	illegal register address
31-8	reserved

-----H-mFEE00300-----

MEM FEE00300h - Pentium + - LOCAL APIC - INTERRUPT COMMAND REGISTER (ICR)

Size: DWORD

Note: this is the low half of the 64-bit ICR

SeeAlso: MEM FEE00310h,#M0121

Bitfields for Pentium APIC Interrupt Command Register:

Bit(s) Description (Table M0121)

7-0	interrupt vector number
10-8	delivery mode (see #M0122)
11	destination mode
12	delivery status (read-only) 1 = transfer pending
13	reserved
14	level (0 = INIT Level Deassert message, 1 = anything else)
15	trigger mode (1)
17-16	remote read status (read-only)
19-18	destination shorthand

00 as specified by destination field
 01 self
 10 all including self
 11 all except self
 55-20 reserved
 63-56 destination for interrupt request or message
 SeeAlso: #M0124

(Table M0122)

Values for Pentium APIC delivery mode:

000b fixed
 001b lowest-priority
 010b SMI
 011b remote read
 100b NMI
 101b INIT
 110b start up
 111b reserved

SeeAlso: #M0121

-----H-mFEE00310-----

MEM FEE00310h - Pentium + - LOCAL APIC - INTERRUPT COMMAND REGISTER (ICR)

Size: DWORD

Note: this is the high half of the 64-bit ICR

SeeAlso: MEM FEE00300h,#M0121

-----H-mFEE00320-----

MEM FEE00320h - Pentium + - LOCAL APIC - LOCAL VECTOR TABLE ENTRY 0 (TIMER)

Size: DWORD

SeeAlso: MEM FEE00350h, MEM FEE00370h, MEM FEE003E0h, INT 70h

Bitfields for Pentium APIC timer local vector entry:

Bit(s)	Description	(Table M0123)
7-0	interrupt vector number	
11-8	reserved	
12	delivery status (read-only)	
	1 = interrupt being sent to APIC	
15-13	reserved	
16	interrupt delivery disabled	
17	timer mode (0=one-shot, 1=periodic)	
31-18	reserved	

SeeAlso: #M0125,#M0124

-----H-mFEE00330-----

MEM FEE00330h - Pentium + - LOCAL APIC - RESERVED

SeeAlso: MEM FEE00000h

-----H-mFEE00340-----

MEM FEE00340h - Pentium + - LOCAL APIC - RESERVED

SeeAlso: MEM FEE00000h

-----H-mFEE00350-----

MEM FEE00350h - Pentium + - LOCAL APIC - LOCAL VECTOR TABLE ENTRY 1 (LINT0)

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Size: DWORD

SeeAlso: MEM FEE00320h, MEM FEE00360h

Bitfields for Pentium APIC LINTx local vector entry:

Bit(s)	Description	(Table M0124)
7-0	interrupt vector number	
10-8	delivery mode	
	000 fixed	
	100 NMI	
	111 external interrupt (8259A-compatibility)	
11	reserved	
12	delivery status (read-only)	
	1 = interrupt being sent to APIC	
13	interrupt pin is active low	
14	remote IRR	
15	trigger mode	
	0 edge-sensitive	
	1 level-sensitive	
16	interrupt delivery disabled	
31-17	reserved	

SeeAlso: #M0123

-----H-mFEE00360-----

MEM FEE00360h - Pentium + - LOCAL APIC - LOCAL VECTOR TABLE ENTRY 2 (LINT1)

Size: DWORD

SeeAlso: MEM FEE00350h, MEM FEE00370h, #M0124

-----H-mFEE00370-----

MEM FEE00370h - Pentium + - LOCAL APIC - LOCAL VECTOR TABLE ENTRY 3 (Error)

Size: DWORD

SeeAlso: MEM FEE00320h, MEM FEE00370h

-----H-mFEE00380-----

MEM FEE00380h - Pentium + - LOCAL APIC - INITIAL COUNT REGISTER (ICR) TIMER

Size: DWORD

Desc: timer start value, which together with the Divide Configuration Register also determines its period when periodic mode has been selected

SeeAlso: MEM FEE00000h, MEM FEE00390h

-----H-mFEE00390-----

MEM FEE00390h - Pentium + - LOCAL APIC - CURRENT COUNT REGISTER (CCR) TIMER

Size: DWORD

Desc: current timer count; when this value reaches zero, an interrupt is generated

Note: read-only

SeeAlso: MEM FEE00380h

-----H-mFEE003A0-----

MEM FEE003A0h - Pentium - LOCAL APIC - RESERVED

SeeAlso: MEM FEE00000h

-----H-mFEE003B0-----

MEM FEE003B0h - Pentium - LOCAL APIC - RESERVED

SeeAlso: MEM FEE00000h

-----H-mFEE003C0-----

MEM FEE003C0h - Pentium - LOCAL APIC - RESERVED

SeeAlso: MEM FEE00000h

-----H-mFEE003D0-----

MEM FEE003D0h - Pentium - LOCAL APIC - RESERVED

SeeAlso: MEM FEE00000h

-----H-mFEE003E0-----

MEM FEE003E0h - Pentium + - LOCAL APIC - TIMER DIVIDE CONFIGURATION REGISTER

Size: DWORD

SeeAlso: MEM FEE00000h, MEM FEE00320h

Bitfields for Pentium (and later) APIC timer divide configuration:

Bit(s) Description (Table M0125)

31-4 reserved

3,1,0 divisor

000 divide by 2

001 by 4

010 by 8

...

110 by 128

111 by 1

2 zero (0)

Note: the divisor determines the timer's time base relative to the processor clock


SeeAlso: #M0123

-----MFFFF0010-----

MEM FFFFh:0010h - HIGH MEMORY AREA (HMA)

Size: 65520 BYTES

71.5 Other resources

Wonderful documents on CMOS RAM, Far call interface list, Model Specific Registers, Assembler Opcodes, I2C Bus devices and System-management mode are part of RBIL. Because of space constraint I avoid listing them here. Anyhow they are available on CD .